COPY OF CLAIMS SUBMITTED ON 04/17/03

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1. (Twice Amended) A method of fabricating a CMOS inverter comprising:

providing a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer, the heterostructure comprising a planarized surface located between the strained surface layer and the Si substrate and having a surface roughness less than 1 nm, whereby the strained surface layer also exhibits a roughness less than 1 nm; and

integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

CLEAN COPY OF ALL PENDING CLAIMS

1. (Twice Amended) A method of fabricating a CMOS inverter comprising:

providing a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer, the heterostructure comprising a planarized surface located between the strained surface layer and the Si substrate and having a surface roughness less than 1 nm, whereby the strained surface layer also exhibits a roughness less than 1 nm; and

integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

4. The method of claim 1, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

5. The method of claim 1, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

6. The method of claim 1, wherein the strained surface layer comprises Si.

7. The method of claim 1, wherein $0.1<x<0.5$.

8. The method of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in bulk silicon.

9. The method of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in the strained surface layer.

10. The method of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in bulk silicon.

11. The method of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in the strained surface layer.

12. The method of claim 7, wherein the gate drive is reduced to lower power consumption.

13. (Amended) A method of fabricating an integrated circuit comprising:

providing a heterostructure having a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strain d layer on said relaxed $Si_{1-x}Ge_x$ layer;

planarizing a surface between the strained layer and the Si substrate to a surface roughness less than 1 nm; and

forming a p transistor and an n transistor in said heterostructure, wherein said strained layer comprises the channel of said n transistor and said p transistor, and said n transistor and said p transistor are interconnected in a CMOS circuit.

16. The method of claim 13, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

17. The method of claim 13, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

18. The method of claim 13, wherein the strained layer comprises Si.

19. The method of claim 13, wherein $0.1<x<0.5$.

20. The method of claim 13, wherein the CMOS circuit comprises a logic gate.

21. The method of claim 13, wherein the CMOS circuit comprises a NOR gate.

22. The method of claim 13, wherein the CMOS circuit comprises an XOR gate.

23. The method of claim 13, wherein the CMOS circuit comprises a NAND gate.

24. The method of claim 13, wherein the p-channel transistor serves as a pull-up transistor in said CMOS circuit and the n-channel transistor serves as a pull-down transistor in said CMOS circuit.

25. The method of claim 13, wherein the CMOS circuit comprises an inverter.

26. A method of fabricating a CMOS inverter comprising:

providing a graded $Si_{1-x}Ge_x$ layer on a first Si substrate;

providing a relaxed $Si_{1-y}Ge_y$ layer on said graded layer to form a first structure;

bonding said relaxed layer of said first structure to a second structure that includes a second Si substrate;

removing said first Si substrate and said graded layer;

providing a strained surface layer on said relaxed layer to form a heterostructure; and

integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

27. A method of fabricating an integrated circuit comprising:

providing a graded $Si_{1-x}Ge_x$ layer on a first Si substrate;

providing a relaxed $Si_{1-y}Ge_y$ layer on said graded layer to form a first structure;

bonding said relaxed layer of said first structure to a second structure that includes a second Si substrate;

removing said first Si substrate and said graded layer;

providing a strained surface layer on said relaxed layer to form a heterostructure; and

forming a p transistor and an n transistor in said heterostructure, wherein said strained layer comprises the channel of said n transistor and said p transistor, and said n transistor and said p transistor are interconnected in a CMOS circuit.